A Simulation Based Analysis of Lowering Dynamic Power in a CMOS Inverter

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Abstract— With the increase in demand of high fidelity portable devices, there is more and more emphasis laying down on the development of low power and high performance systems. In the next generation processors, the low power design has to be incorporated into fundamental computation units, such as adder. CMOS circuit design plays a crucial role in designing of these computation units (like adder and multiplier) so if there is any optimal way to reduce the power dissipation in CMOS circuits then it will directly lower down the power dissipation of other circuits and logic gates as well. In this paper we have studied and analyzed different techniques to reduce the dynamic power of CMOS circuit with the help of performing simulation on some significant factors (i.e device characteristics) of respective circuitry designs by using Cadence-Virtuoso tool.

Index Terms— Low dynamic power, CMOS circuits, Cadence-Virtuoso, Device Characteristics.

I. Introduction

As the size of the transistors getting reduced with increased complexity, the power dissipation of the circuit design has been given an important pace. With billions of transistors incorporated on single chip, many crucial issues are emerging at faster rate such as handling the power consumption by these CMOS circuits. The average power consumption in CMOS digital is expressed as:

$$P_{avg} = P_{dynamic} + P_{short\text{-}circuit} + P_{leakage} + P_{static} \quad (1)$$

Our area to work on is to concentrate on reducing the dynamic power of CMOS. Dynamic power represents the power dissipated during a switching event i.e. when the output node voltage of a CMOS logic gate makes a logic transition. The switching power is dissipated when energy is drawn from the power supply to charge up the output node capacitance as shown in Figure 1. During charge up phase, the output node voltage typically makes a full transition from 0V to < V_{DD} and one half of the energy drawn from power supply is dissipated as heat in the conducting PMOS transistors and no energy is drawn from the power supply during discharging phase yet the energy stored in the output capacitor during charge up is dissipated as heat in the conducting NMOS transistors, as the output voltage drops from V_{DD} to > 0V as shown in Figure 2.

The average dynamic power consumption in CMOS logic circuits:

$$Pavg = (\alpha Ti \times Ci \times Vi)\, V_{DD} \times fclock \quad (2)$$

Where, Ci = parasitic capacitance associated with each node in the circuit, αTi = corresponding node transition factor associated with the node.

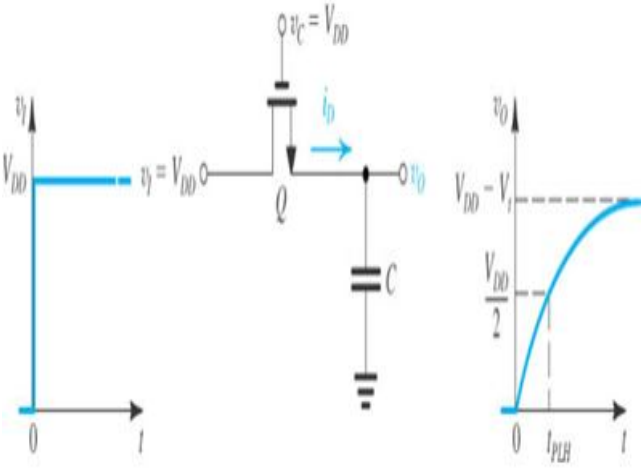

Figure 1. Charging of capacitor [1]

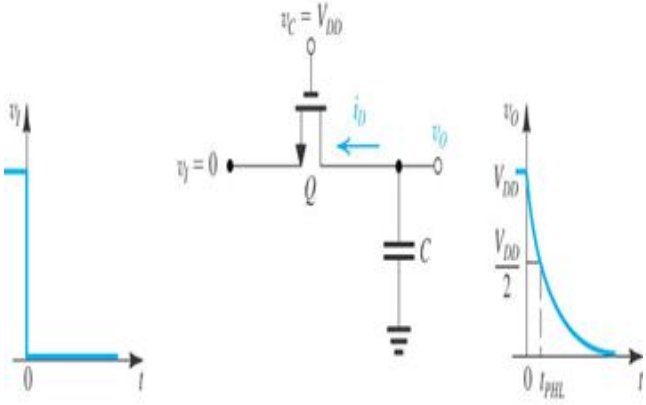

Figure 2 Discharging of capacitor[1]

Hence the term in parenthesis represents the total no of charge which is drawn from the power supply during each switching event [2] .Since the dynamic power is the most dominating component of the total power consumption so reducing its value to a optimum level will bring the design of circuit to more improvised and modified level.

From Equation(2)[2] it can be analyzed that the average dynamic power can be decreased by either decreasing V_{DD} or fclock We are going to discuss and analyze by taking V_{DD} as parameter to reduce the power dissipation and check out its influence on complete design. Although the reduction of power supply voltage significantly reduces the dynamic power dissipation, the inevitable design trade-off is increase in of delay.

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$$\tau_{PHL} = \frac{C_{load}}{k_n(V_{DD} - V_{T,n})}\left[\frac{2V_{T,n}}{V_{DD} - V_{T,n}} + ln\left(\frac{4(V_{DD} - V_{T,n})}{V_{DD}} - 1\right)\right]$$

$$\tau_{PLN} = \frac{C_{load}}{k_p(V_{DD} - |V_{T,p}|)}\left[\frac{2|V_{T,p}|}{V_{DD} - |V_{T,p}|} + ln\left(\frac{4(V_{DD} - |V_{T,p}|)}{V_{DD}} - 1\right)\right] \quad (3)$$

From Equation (3)[2] we can analyze that the negative effect of reducing the power supply voltage upon delay can be compensated for, if the threshold voltage (V_T) of transistors is scaled down accordingly.

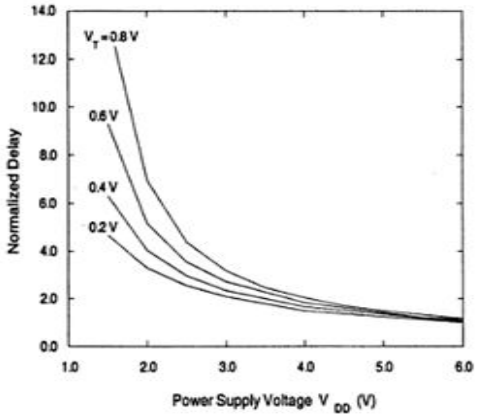

Figure 3 Norm alised Delay Vs power Supply Voltage[1]

When threshold voltage is scaled down linearly, it allows the circuit to produce the same speed performance at a lower V_{DD} but the threshold voltage may be scaled down to some extent only due to problems arising after that which are sub threshold voltage or noise margin as shown in Figure 3.

II. Techniques Used In Reducing The Dyanamic Power

A. *Voltage Bootstrapping*

Voltage Bootstrapping is a very useful technique which is used to overcome threshold voltage drops in digital circuits. The operation speed is improvised at low supply voltage region for driving a large capacitive load by boosting internal nodes beyond the power supply or below the ground using a single bootstrap capacitor. Since the charge loss is eliminated from the bootstrap nodes in this technique, the bootstrap voltages are more than the conventional CMOS bootstrap circuit. [3]. Referring to Figure 4, and assuming the logic '0' at input 'V_{in}', the transistor M1 will turn off and the output voltage 'V_{out}' will start to rise. This change in the output voltage level will now be coupled to V_x through the bootstrap capacitor, C_{boot}.

Therefore, the transient current Icboot flowing through the capacitor Cboot is

$$I_{cboot} = C_{boot}\{d(V_{out} - V_x)/dt\} \quad (4)$$

An extra "dummy " transistor is typically added to increase the bootstrap capacitance (C_{boot}). Since, its drain and Source terminals are connected together, the dummy transistor acts as an MOS capacitor between V_x and V_{out}. Although this circuit arrangement contains two additional transistors to achieve voltage bootstrapping, the resulting circuit performance improvement is usually well worth the extras silicon used for

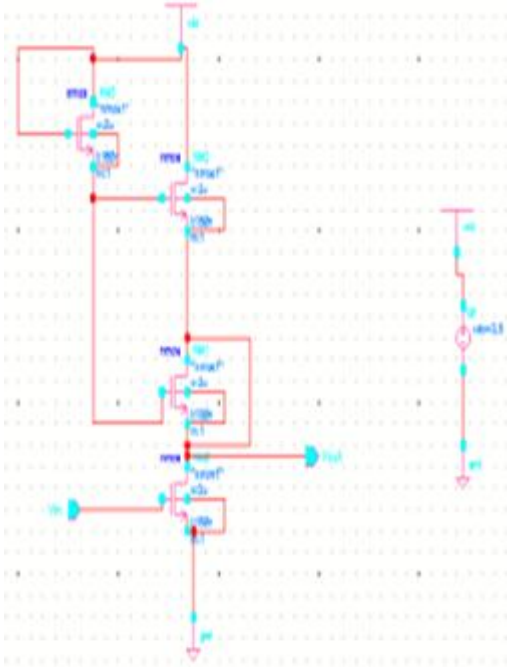

Figure 4 Shematic Diagram for Voltage Bootstrapping

bootstrapping devices. The simulation using Cadence spectra shows the following results as shown in Table.1 and in Figure 5.

Table I. Power Consumption In Voltage Bootstrapping Technique

Power	Average Power (W)	Static Power (W)	Dyanamic Power (W)
Values	$82.71x10^{-6}$	$57.84x10^{-12}$	~$82.71x10^{-6}$

B. *NORA Logic*

In order to maintain high switching speed at low supply voltages it is necessary to reduce the transistor threshold voltage, V_T, in proportion [4]. For supply voltages much below 1V the value of V, may be just tens or hundreds of millivolts, and the subthreshold leakage current of these transistors becomes significant [5].

The main building blocks of NORA technique are shown in Figure 6. The logic functions are implemented using n-type and p-type dynamic CMOS and C^2MOS blocks. Conventional (static) CMOS function blocks can also be eventually employed[6]. As it will further be shown, to guarantee a fully racefree operation[3] in pipelined circuits, the storage of information must always be performed by a C^2MOS function block (C^2MOS latch stage). For pulse voltage 1.8V from clock changing from 0 to 1, the section is in the precharge phase. The outputs of all the n- and p-dynamic blocks are precharged to "1" and "0," respectively. Also during this phase, the phase section inputs are in a sampling mode, i.e, these inputs are set up. For phase 1 to 0, the phase section is in the evaluation phase.The simulation using Cadence spectra shows the following results as in Table 2 and in Figure 7.

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Figure 5 Average Power Consumption in Voltage Bootstrapping Technique

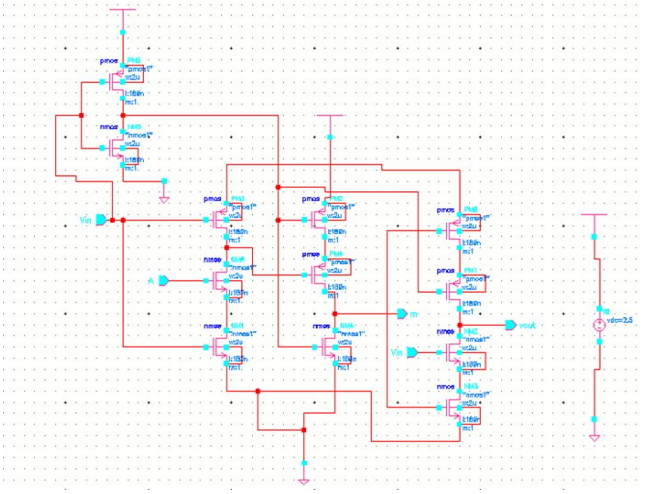

Figure 6 Schematic Diagram for NORA logic

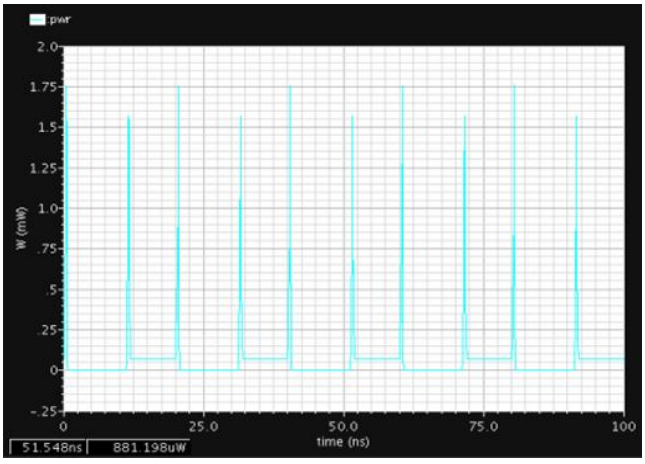

Figure 7 Average Power Consumption in NORA logic

C. Multiple-Threshold CMOS (MTCMOS) Logic

The MTCMOS technique was first introduced in SOI technology in [7], [8], in which the gate of the MOSFET is connected to its substrate. MTCMOS shows a lot of advantages over the conventional CMOS logic in the sub

TABLE. II. POWER CONSUMPTION IN NORA LOGIC

Power	Average Power (W)	Static Power (W)	Dyanamic Power (W)
Values	$1.513x10^{-3}$	$48.84x10^{-12}$	$\sim 1.513x10^{-3}$

threshold region in terms of speed and energy savings[9].In this technique, two transistors (both pMOS and nMOS) are based on two different threshold voltages in the circuit as shown in Figure 8.

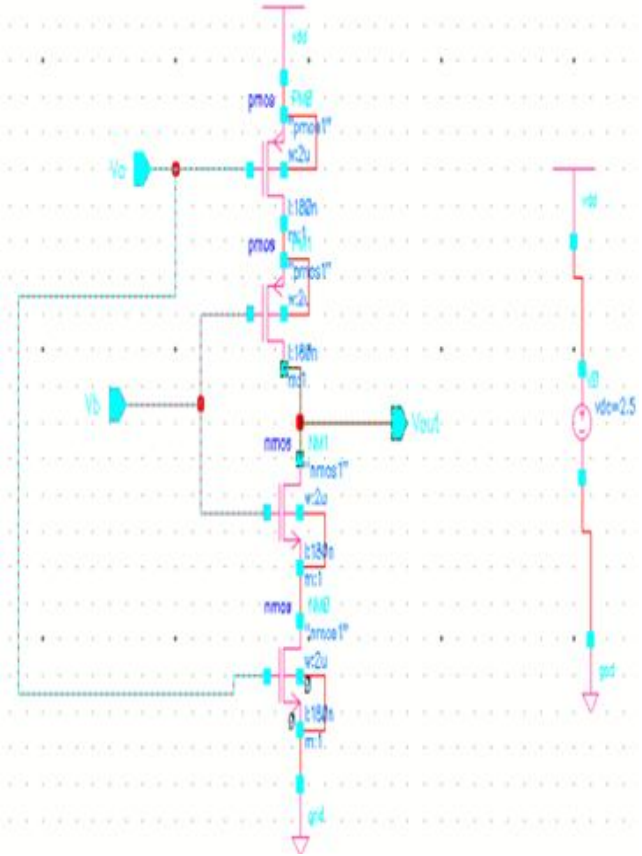

Figure 8 Schematic Diagram for MTCMOS logic

The result of simulation using Cadence spectra shown in the Table 3 and in Figure 9.

TABLE III. POWER CONSUMPTION IN MTCMOS LOGIC

Power	Average Power (W)	Static Power (W)	Dyanamic Power (W)
Values	$2.515x10^{-6}$	$7.284x10^{-12}$	$\sim 2.515x10^{-6}$

D. Replacement of MOSFETs with CNTFETs

Nanotechnology is a new field of research that cuts across many fields – electronics, chemistry, physics, and biology, that analyses and synthesizes objects and structures in the Nano scale (10-9 m) such as Nano particles, nanowires, and Carbon Nanotubes (CNTs)[10]. CNT is one of the several cutting-edge emerging technologies within nanotechnology with high efficiency and a wide range of applications in many different streams of science and technology. Nano-circuits which are based on CNTs such as CNT Field Effect Transistors (CNTFETs) show big promise of less delay and power

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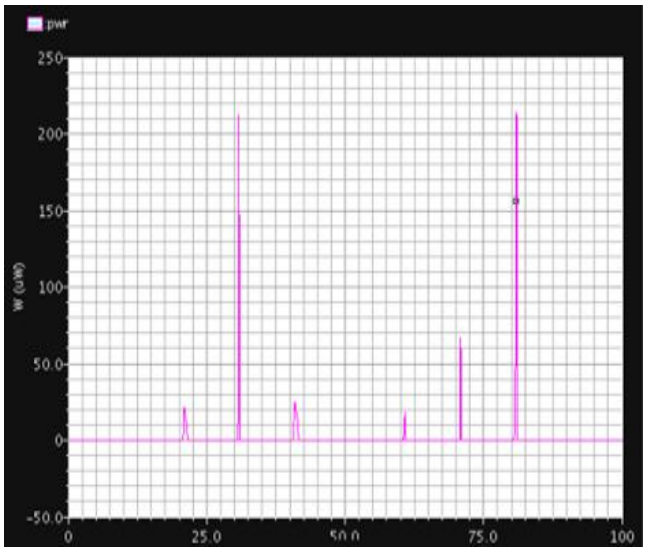

Figure 9 Average Power Consumption in MTCMOS logic

consumption than available silicon-based FETs. Many works and circuit designs through CNTFET have been proposed by CNTFET researchers.

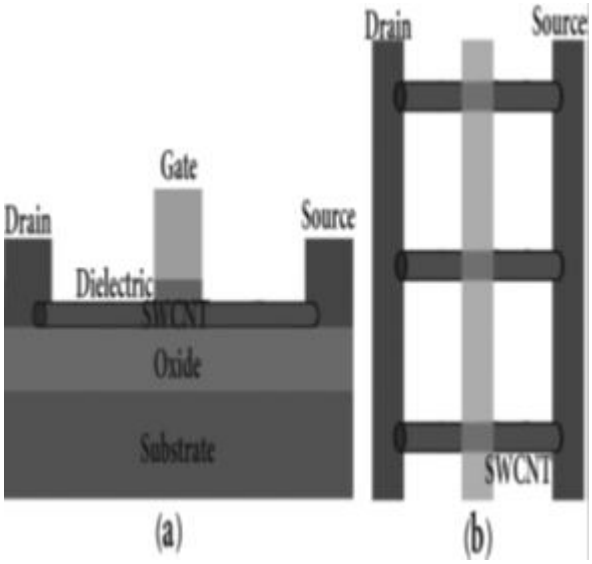

Figure 10 Schematic diagram of a CNTFET: (a) Cross section view (b) top view [10]

According to the simulation results performed by researchers[11], their CNTFET-based design has 75.01%, 7.76% and 76.92% improvement than MOSFET implementation in term of delay, average power and PDP respectively.SWCNT (Figure 10) have many benefits rather than silicon transistors counterpart such as high density of on current and moderately high Ion/Ioff ratio that has many effects on transistors behavior, molecular size, high theoretical transition frequency and changeable threshold voltage depending on carbon nanotube diameter which is an important characteristic of CNTFETs.

Although CNT has been grown into several forms, CNT use is still limited as compared to other wide spread technologies [12]. This is mainly due to:

- It is still difficult to exactly control CNT growth into desired forms, and
- CNT growth is still very expensive due to the low yield of CNTs.

III. Conclusion

Based on the simulation result on various techniques used to lower down the dynamic power of CMOS design, we have concluded that Voltage Bootstrapping technique consumes much power than NORA logic and MTCMOS (Multi-Threshold CMOS) techniques and moreover a new design can be developed by implementing CNT (carbon nano tube) in channel region in traditional MOSFET structure, which improves the power consumption behavior of traditional CMOS structure by nearly 7%.

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